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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,900	12/30/2003	Il-Goo Kim	8028-39 (SPX200211-0051US	7438

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EXAMINER	
LEE, CALVIN	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,900	KIM et al.	
	Examiner	Art Unit	
	Lee, Calvin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-12,14-24 and 26-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-12,14-24 and 26-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment of claims 1, 14, 15, 18, 26, 27, the cancellation of claims 2-4, 13, 25 and the addition of claim 32 (all stated in the Remark dated September 24, 2004) are acknowledged.

Claim Objections

2. Claims 1, 18, 27, and 32 are objected to because of the following informalities:

Claims 1, 18, and 32, line 3, replace "on a semiconductor" with --over a semiconductor--

Claim 1, line 10, replace "antireflective layer" with --the anti-reflective layer--

Claim 27, line 4, replace "antireflective layer" with --anti-reflective layer--

Claim32, line 18, replace "via etch stop" with --via etch stop layer--

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 5-12, 14-24, and 26-32 are rejected under 35 U.S.C. 103(**a**) as being unpatentable over *Kennedy et al (US 6,812,131)* or *Chung et al (US 6,787,448)*, in view of *Arita et al (US 2004/0036076)*.

a) *Kennedy et al* discloses a method of forming a via contact structure, comprising the steps:

-forming a lower interconnection line on a semiconductor substrate **200** [col. 4, ln.25]

-sequentially forming an inter-metal dielectric layer and a hard mask layer **205** on the substrate, wherein the inter-metal dielectric layer comprises a trench etch stop layer **203** sandwiched between lower and upper inter-metal dielectric films **203**, **204** [Fig. 2a]

-patterning the hard mask layer and the inter-metal dielectric layer to form a via hole **207** [Fig. 2c]

-forming a sacrificial layer **208** filling the via hole on the hard mask layer [Fig. 2d]

-patterning the sacrificial layer and the hard mask layer to form a first sacrificial layer pattern having an opening **210** that crosses over the via hole and a second sacrificial layer pattern that remains in the via hole **207**, and to *simultaneously* form a hard mask pattern underneath the first sacrificial layer pattern (i.e., the two portions of the layer **208**) [Fig. 2e and col. 5]

-partially etching the inter-metal dielectric layer using the hard mask pattern as an etching mask to form a trench crossing over the via hole [Fig. 2f and col. 6]
-removing the second sacrificial layer pattern to expose the lower interconnection line [Fig. 2g]
-forming an upper metal layer by stacking a diffusion barrier **211** and a metal layer **212** [Fig. 2h]
-planarizing the upper metal layer to form an upper metal interconnect line [Fig. 3i]

Kennedy et al also suggests: the inter-metal dielectric layers "may be form from organic dielectrics" [col. 4, ln.43]; the trench etch stop layer "is typically silicon oxide deposited by CVD, but may be other dielectric materials" [col. 3, ln.57]; the hard mask layer "is typically silicon oxide or silicon oxynitride... Other dielectric materials and other deposition methods may be used to form hardmask layer" [col. 5, ln.1]; the sacrificial layer is "inorganic dielectric" [col. 6, ln.18].

Since *Kennedy et al* discloses, "the sacrificial inorganic dielectric may incorporate an ultraviolet light absorbing dye," the sacrificial layer may also function as an anti-reflective layer. In other words, sacrificial layer **208** may comprise an ARC sublayer on a sacrificial sublayer. Nevertheless, such anti-reflective layer on a sacrificial layer is known in the semiconductor photolithography art as evidenced by *Arita et al* disclosing "the second anti-reflective film **13**, SOG sacrificial film **12**, first hard mask **6** and interconnect interlayer film **5** are dry-etched selectively, one after the other, using the second photoresist **11** as the etching mask until the etching stopper film **4** is exposed [Fig. 2F and ¶0059].

Furthermore, both *Kennedy et al* and *Arita et al* are directed to achieving a the same structure and thus one with ordinary skill in the specific art would recognize the interchangeability of the process steps and be able to combine the two inventions with an expectation of success.

It would have been obvious to one with ordinary skill to have modified the via structure of *Kennedy et al* by utilizing an ARC covering an existing sacrificial layer for the purpose of producing a light absorbing background that ensures uniform reflectivity of light used to expose the photoresist during trench patterning.

b) In re claim 30, *Kennedy et al* is silent about the hard mask layer being removed during or after the planarization step. While *Kennedy et al* discloses the removal of the hard mask layer prior to the filling of the trench, this limitation is rendered obvious to one with ordinary skill in the specific art to remove the hard mask layer during or after the planarization step solely in light of *Kennedy et al* since in general the transposition of process steps or the splitting of one step into

two, where the processes are substantially identical or equivalent in terms of function, manner and result, was held to not patentably distinguish the processes. *Ex parte Rubin*, 128 USPQ 159.

c) *Chung et al* discloses a method of forming a via contact structure, comprising the steps:
-forming a lower interconnection line **305** over a semiconductor substrate **300** [col. 5]
-sequentially forming an inter-metal dielectric layer and a hard mask layer **340** on the substrate, wherein the inter-metal dielectric layer comprises a trench etch stop layer **323** sandwiched between lower and upper inter-metal dielectric films **331**, **333** [Fig. 3A]
-patterning the hard mask layer and the inter-metal dielectric layer to form a via hole **360** [Fig. 3B]
-forming a sacrificial layer **370** filling the via hole on the hard mask layer [Fig. 3C]
-patterning the sacrificial layer and the hard mask layer to form a first sacrificial layer pattern having an opening **365** that crosses over the via hole and a second sacrificial layer pattern **375** that remains in the via hole, and to *simultaneously* form a hard mask pattern **340** underneath the first sacrificial layer pattern (i.e., the two end portions of the layer **370**) [Fig. 3D]
-partially etching the inter-metal dielectric layer using the hard mask pattern as an etching mask to form a trench **365** crossing over the via hole **360** [col. 6, ln.5]
-removing the second sacrificial layer pattern to expose the lower interconnection line [Fig. 3I]
-forming an upper metal layer **390** having a diffusion barrier **391** and a metal layer **393** [Fig. 3J]
-removing the hard mask layer during a planarization step of the upper metal layer to form an upper interconnect line [col. 6, ln.58]

Chung et al also suggests: the inter-metal dielectric layers "comprise a doped oxide such as HSQ, MSQ, and SiOC" [col. 5, ln.35]; the trench etch stop layer "comprise a material having an etch selectively relative to the first and second interlayer insulating layers **331** and **333**, for example, a nitride film" [col. 5, ln.39]; the hard mask layer "acting as a buffer layer in CMP process, for example a PEOX" [col. 5, ln.44]; the sacrificial layer "is comprised of a flowable oxide such as HSQ" [col. 5, ln.65].

Chung et al is silent about an anti-reflective layer. *Arita et al* discloses "the second anti-reflective film **13**, SOG sacrificial film **12**, first hard mask **6** and interconnect interlayer film **5** are dry-etched selectively, one after the other, using the second photoresist **11** as the etching mask until the etching stopper film **4** is exposed [Fig. 2F and ¶0059].

Response to Arguments

5. Applicants argued that "neither *Chung* nor *Nagahara* teach or suggest a method of forming a via contact structure comprising forming an anti-reflective layer on a sacrificial layer." Examiner takes the position that Applicants disclose, "the sacrificial layer **21** may be formed of an inorganic material layer or organic material layer" [¶ 0028]. Those recognized dielectric materials are therefore interchangeable with the organic low-k dielectric layer (i.e., the sacrificial layer) [see Fig. 1B of *Chung et al*] and the cap film 3 of silicon dioxide being coated with anti-reflection film [see ¶ 0050 of *Nagahara et al*]. Therefore, Applicants' arguments filed on September 24, 2004 have been fully considered but they are not persuasive.

After a closer review of the arguments and after further search related arts, the examiner has found new pieces of art, which would read on the applicant's claims. Therefore, above is a new ground of rejections. The new feature "anti-reflective layer on the sacrificial layer" found in the amended claims and the additional claim put this Office Action to be a FINAL action.

6. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire three months from the mailing date of this action. In the event a first reply is filed within two months of the mailing date of this final action and the advisory action is not mailed until after the end of the three-month shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than six months from the date of this final action.

Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896, Monday to Thursday, from 7 to 5 (ET). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2825's Supervisory Patent Examiner *Matthew Smith* whose telephone number is (571) 272-1907.

Any inquiry relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0596. The central fax number is (703) 872-9306 for all communications to be entered (e.g., amendments, remarks, IDS, etc.)

December 9, 2004

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